## REMARKS/ARGUMENTS

Claims 1-25 were pending in the present application. By virtue of this response, Claims 16 and 25 have been amended. Accordingly, Claims 1-25 are currently under consideration. Amendment of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added. The claim amendments here are not narrowing.

**Rejections**

The Examiner rejected Claim 16 under 35 U.S.C. §112, second paragraph, saying it is unclear what is meant by a (2N order) resonator. In response, Claim 16 and similarly Claim 25 are amended only to make the claim clearer typographically. Hence this is not a narrowing amendment. The amendment shows that the characters "2N" are meant to represent the value N multiplied by the value 2. This reads on page 7, paragraph 36 stating that the resonator is an even phase, e.g. two phase resonator.

Claims 1-7 stand rejected under 35 U.S.C. §103 as unpatentable over Pellon in view of Abbey. The Examiner points to Pellon Fig. 8 and admits that "Pellon does not specifically teach an odd-phase sample-and-hold circuit coupled to a first node of the analog-to-digital converter. However, Abbey...teaches in figure (4) a ...converter that includes sample-and-hold circuits (400) coupled to the input of a first node of the circuitry to hold data prior to processing." Since the Examiner did not further comment on the other claims but rejects all claims, it is assumed that the remaining claims were also rejected citing these two references under §103. If the Examiner intended other than to reject all pending claims under §103, it would be appreciated if he would so indicate.

Traversal of §103 Rejection

The §103 rejections are traversed. It is respectfully submitted that the two cited references, even in combination, fail to meet the present claims and therefore the rejection is

*prima facie* inadequate, and it is requested that it be reconsidered and withdrawn for the reasons set forth hereinafter.

First as understood by the Examiner, the mere use of a sample and hold circuit at the input of an analog-to-digital converter is well known, see for instance present Fig. 1a (labeled "prior art") which shows the sample and hold circuit 10 as the input element to the modulator 3. See also the present specification at page 1 under "Related Art" at paragraph 4 which states:

> By way of illustration, switched capacitor circuits are used in the known delta-sigma analog-to-digital converter (ADC) that is implemented with multi-phased sample-and-hold (S/H) circuits and multi-phased resonators.

Therefore, there was no indication that the mere presence of a sample and hold circuit at the input portion of a modulator was intended by itself to be inventive.

Instead, Claim 1 is directed to the modulator having a sample and hold circuit which is, as recited in the second line of Claim 1, an "odd-phase sample and hold circuit" combined with, in line 4 of Claim 1, "an even-phase resonator."

As further stated in paragraph 35 of the specification at page 7:

> Embodiments of the present invention, described in greater detail below, overcome challenges to providing high speed, high performance, delta-sigma ADCs by incorporating a low distortion aspect into the delta-sigma ADC, and by providing phases for the S/H circuit and resonator as described herein. (emphasis added.)

Continuing at paragraph 36:

> Various embodiments provide a band-pass delta-sigma ADC modulator including the low distortion aspect shown in Fig. 5. An odd-phase (e.g. single-phase or 3-phase) S/H circuit 30 is employed with an even-phase (e.g. two-phase) resonator 34. An odd-phase S/H circuit 30 assures that S/H spurious signals are out-of-band. Two-phased resonator 34 reduces or eliminates the in band noise

degradation are to resonator component mismatches.

Fig. 6 shows the spectrum at the output of the low distortion delta-sigma ADC modulator of Fig. 5. This is superior to the spectrum shown in prior art Figures 2 through 4 because none of them meet the desirable goal of simultaneously low spurs and low noise, in terms of the low spurs being out of band. In Fig. 6 the frequency band of interest is labeled "signal of interest" indicating a particular frequency band. The particular combination of phases of the sample and hold and the resonator in Claim 1 are recited in combination with the two feed forward stages also shown in Fig. 5, the first being the feed forward stage 46 and the other being the feed forward stage 40.

It is respectfully submitted that the two references, alone or even in combination, further combined with, for instance, the admitted prior art of present Fig. 1a, fail to meet present Claim 1. Taking Pellon as the primary reference, the Examiner identified the feed forward stages as being in Pellon. However, he admitted there is no sample and hold circuit in Pellon. Moreover, Pellon is not specific about the phases of his resonator. For instance, Pellon Fig. 8b shows some unknown number of resonators but with no accompanying discussion of phase. There appears to be no discussion in Pellon of the spur/noise tradeoff addressed in accordance with the present invention.

The Examiner cited then as the secondary reference Abbey to make up the admitted deficiency in terms of the sample and hold circuit being absent from Pellon. However as pointed out above, use of sample and hold circuits on the input of an ADC modulator is well known, see present Fig. 1a. Moreover, it is not clear why one would substitute the sample and hold circuits shown in Abbey into Pellon since apparently the sample and hold circuits in Abbey are not used for sampling and holding as in present Fig. 1a but instead provide the resonator-type function. Note that there are no other components shown in Fig. 4 of Abbey that would perform the resonator function. Moreover, the sample and hold circuits are identified as "differentiators" in Abbey, see Abbey col. 6, beginning line 10:

> FIG. 4 depicts a two stage synchronously sampled, high path delta-sigma modulator based ADC architecture. The high pass modulator creates a single pass band extending down in frequency from the Nyquist frequency ... and shifts quantizer noise down in frequency

> away from the pass band. In the high pass modulator, the serial cascade of stages are differentiators (integrator stages are used in the low pass modulators). The architecture of FIG. 4 is called a "two stage" converter since it includes a first stage differentiator 400 and a second stage differentiator 402. Other embodiments of the delta-sigma high fast modulator can include one stage or more than two stages. (emphasis added.)

Hence these stages appear to fulfill the function in Pellon of the resonators, which also can have N number of stages, rather than the sample and holding function of the input circuit. Hence in this sense Abbey brings less in terms of significance to the rejection than does prior art Fig. 1a which of course, even in combination with Pellon, fails to meet the present claims.

Moreover, Abbey is not specific about the phases of the sample and hold circuits 400, 402 in his Fig. 4 and hence fails to meet Claim 1 in this regard.

Moreover, even if arguendo one were to combine Pellon with Abbey in an attempt to meet Claim 1, the resulting combination still fails to meet Claim 1. That is, there is still no combination in Pellon and Abbey of odd-phase sample and hold with even-phase resonators. There are either no sample and holds because (1) Abbey shows sample and holds 400, 402 as being effectively resonator stages, or (2) if there are sample and holds in Abbey, there are four of them. There is still no indication in either reference of "an odd-phase sample and hold circuit."

Hence the Examiner's suggested combination would provide, at best, a modulator with either no sample, and holds (since Abbey's differentiators 400, 402 would be understood as duplicating Pellon's resonators), or if there are sample and holds, there is no odd-phase sample and hold.

Moreover, neither reference suggests the advantage addressed by the invention since they both fail to solve or even mention the problem of providing the combination of low in-band spurs with low noise. Hence the modulator in accordance with Claim 1 has advantages over the prior art and also over any ADC resulting from the two combined references as suggested by the Examiner. Further, there is no suggestion in either reference or in other references to modify either

reference in order to meet Claim 1, which thereby distinguishes over the references.

The claims dependent upon Claim 1 are Claims 2-16, which it is respectfully submitted distinguish over the references for at least the same reasons as does the base claim.

Additionally, certain of the dependent claims are directed to additional features not shown in either reference. The Examiner failed to specifically reject these dependent claims and hence it is respectfully submitted they additionally distinguish over the references. See for instance Claim 4 which recites "the resonator is a switched capacitor resonator." Pellon discloses resonator 751 of Fig. 8b in further detail at Fig. 7b but it is not seen how this is a switched capacitator resonator. For instance, an exemplary switched capacitator resonator is shown in the present application in detailed schematic form in Fig. 7 at 34. No such structure is shown in either reference, and hence for at least this reason Claim 4 and the claims dependent thereon distinguish thereover.

Independent Claim 17 is a method claim directed to modulating an analog signal and distinguishes over the references, even in combination, at least for reasons similar to those as discussed above in conjunction with Claim 1. Claim 17 recites in its second line "sampling and holding the analog signal using an odd number of phases; applying the sampled and held signal to an even-phase resonator;". Again no such acts are disclosed or suggested, even given the combination of the two cited references, hence Claim 17 distinguishes thereover. Similarly, Claims 18-25, dependent on Claim 17, distinguish over the references for at least the same reasons as does the base claim. Further, Claim 23 recites "configuring the resonator for one of capacitor switching or capacitor flipping." Again no such acts are disclosed or even suggested in the two cited references, and so Claim 23 additionally distinguishes thereover.

Therefore, it is respectfully submitted that all pending claims are allowable and it is requested that the rejection of same be reconsidered and withdrawn.

## CONCLUSION

In view of the above, all pending claims in this application are believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and pass this application to issue. If it is determined that a telephone interview would expedite prosecution, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 549212000200.

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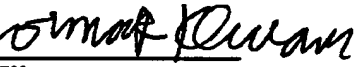
Respectfully submitted,

By 

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